REMARKS

Claims 1-26 are pending at the time of this action, with Claims 1, 11, 18 and 25 being independent. Reconsideration and allowance of the above-referenced application are respectfully requested.

Claims 1, 7, 8, 10, 11, 14, 15, 17, 22 and 24-26 stand rejected under 35 U.S.C. 102(b) as allegedly being anticipated by Ball (U.S. Patent No. 5,615,357). Claims 2-6, 9, 12, 13, 16, 18-21 and 23 stand rejected under 35 U.S.C. 103(a) as allegedly being unpatentable over Ball in view of Krishnaswamy et al. (U.S. Patent No. 6,622,300). These contentions are respectfully traversed.

The Office refers to figure 5A of Ball as the sole basis for rejecting independent claim 1. Figure 5A in Ball shows, "the sequence of events by which a simulator of this invention employs a benchmark program to generate performance statistics." (*See* Ball at col. 9, lines 26-28.) As further described in Ball:

> The benchmark program 50 is executed on a tool such as a fast instruction accurate processor model in such a manner that it generates a trace file 56 containing the information such as that shown in FIG. 4B. […] [T]he trace file 56 is chopped into a number of small segments by a sampler 58. Thereafter, the trace file samples are provided to a cycle accurate simulator 60

> which uses the information contained in the traces, in conjunction with static benchmark program 50, to generate a collection of performance statistics 62. [...] Exemplary performance statistics include the total number of cycles required to execute a benchmark, the average number of cycles to execute an instruction in the benchmark, the number of times that cache was accessed, etc.

(*See* Ball at col. 9, lines 31-55.) These teachings of Ball do not describe the presently claimed subject matter.

Independent claim 1 recites, "sampling machine instructions being performed by a processor; identifying instruction types of the sampled machine instructions; and presenting a metric indicating utilization of the processor by identified instruction types." (Emphasis added.) Ball describes sampling a trace file, not sampling machine instructions being performed by a processor. In addition, the performance statistics described in Ball do not include a metric indicating utilization of the processor by identified instruction types. Krishnaswamy et al. fail to cure these defects in Ball. Thus, independent claim 1 should be allowable over Ball and Krishnaswamy et al.

Dependent claims 2-10 should allowable over Ball and Krishnaswamy et al. based on the above arguments and the additional recitations they contain. For example, dependent claim 7 recites, "selecting the instruction types to be identified from a set of available instruction categories based

on received input." The cited portion of Ball (col. 2, lines 40-43) describes the trace output as including an effective address for some certain classes of instructions. This does not teach or suggest selecting instruction types to be identified from a set of available instruction categories based on received input. Thus, claim 7 should be allowable for at least this additional reason.

Dependent claim 10 recites, "displaying actual processor speed in real time as the speed varies." The cited portion of Ball (col. 2, lines 30-33) states, "The present invention provides methods and systems for accurately determining the performance of processor designs by using execution-driven simulators adapted to run in a trace driven mode." (Emphasis added.) The reference here to "a trace driven mode" clearly indicates that there is no real time display of processor speed in Ball. Thus, claim 10 should be allowable for at least this additional reason.

Independent claim 11 recites, "identifying instruction types of sampled machine instructions being performed by a processor; and presenting a metric indicating utilization of the processor by identified instruction types." (Emphasis added.) For reasons similar to those addressed above, neither Ball nor Krishnaswamy et al. describe identifying instruction types of sampled machine instructions being performed by a processor, and

presenting a metric indicating utilization of the processor by identified instruction types. Thus, independent claim 11 should be allowable over Ball and Krishnaswamy et al. Dependent claims 12-17 should allowable over Ball and Krishnaswamy et al. based on the above arguments and the additional recitations they contain.

Independent claim 18 recites, "a shared memory that receives information corresponding to a subset of machine instructions retired from a processor; and an instruction mix monitor that identifies instruction types based on the information in the shared memory and presents a metric indicating utilization of the processor by identified instruction types." (Emphasis added.) For reasons similar to those addressed above, neither Ball nor Krishnaswamy et al. describe an instruction mix monitor that identifies instruction types and presents a metric indicating utilization of the processor by identified instruction types. Thus, independent claim 18 should be allowable over Ball and Krishnaswamy et al. Dependent claims 19-24 should allowable over Ball and Krishnaswamy et al. based on the above arguments and the additional recitations they contain.

Independent claim 25 recites, "means for monitoring instruction mix in a processor; and means for displaying in real time the monitored instruction mix in the processor." (Emphasis

added.) For reasons similar to those addressed above, neither Ball nor Krishnaswamy et al. describe means for monitoring instruction mix in a processor; and means for displaying in real time the monitored instruction mix in the processor. Thus, independent claim 25 should be allowable over Ball and Krishnaswamy et al. Dependent claim 26 should allowable over Ball and Krishnaswamy et al. based on the above arguments and the additional recitation it contains.

Conclusion

It is believed that all of the pending claims have been addressed. However, the absence of a reply to a specific issue or comment does not signify agreement with or concession of that issue or comment. Because the arguments made above may not be exhaustive, there may be reasons for patentability of any or all pending claims (or other claims) that have not been expressed. Finally, nothing in this paper should be construed as an intent to concede any issue with regard to any claim, except as specifically stated in this paper.

It is respectfully suggested for all of these reasons, that the current rejections are overcome, that none of the cited art teaches or suggests the features which are claimed, and therefore that all of these claims should be in condition for

allowance. A formal notice of allowance is thus respectfully requested.

Please apply the one month extension of time fee, and any other necessary credits or charges, to deposit account 06-1050.

Respectfully submitted,

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